

Abstract

An object of the invention is to discover at the chip level a portion of a high density of contact holes in wires of a large area that becomes a portion where wire defects will occur. In order to achieve this, the area ratio of the total area of wires of the same node to the total area of contact holes in the wires of the same node is limited in a chip layout and wire formation defects are detected by determining whether or not defects exists based on this limitation. Thus, defects are detected wherein the area ratio exceeds the limit at the layout design stage and thereby formation defects such as a disconnection of a wire of a large area, a wire breakdown, a surface peeling due to a hillock or a defective connection between a wire and a contact hole can be avoided.